What is claimed is:

1. An integrated circuit package, comprising:

a semiconductor die electrically connected to a substrate;

a heat sink having a portion thereof exposed to the surroundings of said package;

a thermally conductive element thermally coupled with and interposed between both said semiconductor die and said heat sink, wherein said thermally conductive element does not directly contact said semiconductor die; and

an encapsulant material encapsulating said thermally conductive element and said heat sink such that said portion of said heat sink is exposed to the surroundings of said package.

2. The integrated circuit package of claim 1, wherein said thermally conductive element is substantially shaped as a right rectangular solid.

3. The integrated circuit package of claim 1, wherein a top portion and a side portion of said heat sink are exposed to the surroundings of said package.

4. The integrated circuit package of claim 1, wherein said thermally conductive element is made of a material from the group consisting of alumina, aluminum nitride, beryllium oxide, ceramic material, copper, diamond compound, and metal.

5. The integrated circuit package of claim 1, wherein said integrated circuit package is a ball grid array integrated circuit package.

6. The integrated circuit package of claim 1, further comprising an interface element interposed between said thermally conductive element and said semiconductor die.

7. The integrated circuit package of claim 6 wherein said interface element is made of a polymeric material.

8. The integrated circuit package of claim 1, wherein a distance between said semiconductor die and said thermally conductive element is about five (5) mils or less.

9. The integrated circuit package of claim 1, wherein said semiconductor die is electrically connected to said substrate by direct chip attachment.

10. An integrated circuit package, comprising:

a semiconductor die electrically connected to a substrate;

a heat sink having a portion thereof exposed to the surroundings of said package;

means for thermally coupling said semiconductor die with said heat sink to dissipate heat from said semiconductor die to the surroundings of said package, wherein said means for thermally coupling is interposed between said semiconductor die and said heat sink but does not directly contact said semiconductor die; and

means for encapsulating said thermally conductive element and said heat sink such that said portion of said heat sink is exposed to the surroundings of said package.

11. An integrated circuit package, comprising:

a substrate comprising:

an upper face with an electrically conductive trace formed thereon; and

a lower face with a plurality of solder balls electrically connected thereto, wherein said trace and at least one of said plurality of solder balls are electrically connected;

a semiconductor die mounted on said upper face of said substrate, wherein said semiconductor die is electrically connected to said trace;

a heat sink having a top portion and a plurality of side portions;

a thermally conductive element thermally coupled to but not in direct contact with said semiconductor die, wherein said thermally conductive element is substantially shaped as a right rectangular solid, is interposed between said semiconductor die and said heat sink, and is attached to said heat sink; and

an encapsulant material formed to encapsulate said upper face of said substrate, said semiconductor die, said thermally conductive element and substantially all of said heat sink except said top portion and said side portions of said heat sink.

12. The integrated circuit package of claim 11, further comprising an interface element interposed between said thermally conductive element and said semiconductor die.

13. The integrated circuit package of claim 12, wherein said interface element is in direct contact with said heat sink.

14. The integrated circuit package of claim 12, wherein said interface element is made of a polymer.

15. The integrated circuit package of claim 11, wherein said semiconductor die is mounted on said upper face of said substrate by direct chip attachment.

16. The integrated circuit package of claim 11, wherein a distance between said semiconductor die and said thermally conductive element is about five (5) mils or less.

17. The integrated circuit package of claim 11, wherein said thermally conductive element is made of a material from the group consisting of alumina, aluminum nitride, beryllium oxide, ceramic material, copper, diamond compound, and metal.

18. The integrated circuit package of claim 11, wherein said top portion of said heat sink comprises a plating.

19. The integrated circuit package of claim 18, wherein said plating is made of nickel.

20. The integrated circuit package of claim 1, wherein said integrated circuit package is a ball grid array integrated circuit package.

21. An integrated circuit package, comprising:

a substrate comprising:

means for electrically interconnecting a semiconductor die; and

means for exchanging electrical signals with an outside device;

a semiconductor die attached and electrically connected to said substrate by attachment means;

a heat sink having means for dissipating thermal energy to the surroundings of said package;

means for thermally coupling said semiconductor die to said heat sink to dissipate heat from said semiconductor die to the surroundings of said package, wherein said means for thermally coupling is interposed between said semiconductor die and said heat sink but does not directly contact said semiconductor die; and

means for encapsulating said semiconductor die, said thermally conductive element and said heat sink such that a portion of said heat sink is exposed to the surroundings of said package but is substantially encapsulated.

22. A method of manufacturing an integrated circuit package, comprising:

installing a carrier onto an upper surface of a substrate, wherein said carrier defines a cavity;

attaching a semiconductor die to said upper surface of said substrate within said cavity of said carrier;

aligning an assembly over said semiconductor die, wherein said assembly comprises a heat sink and a thermally conductive element;

resting said assembly on said carrier such that said thermally conductive element does not directly contact said semiconductor die; and

encapsulating said cavity to form a prepackage such that a portion of said heat sink is exposed to the surroundings of said package.

23. The method of claim 22, wherein said assembly is rested on said carrier such that said thermally conductive element and said semiconductor die are separated by a distance of about five (5) mils or less.

24. The method of claim 22, wherein said attaching said semiconductor die to said upper surface of said substrate is by a direct chip attachment.

25. The method of claim 22, further comprising singulating said prepackage to form said package, wherein a top portion and a side portion of said heat sink are exposed to the surroundings of said package.

26. A method of manufacturing an integrated circuit package, comprising:

installing a carrier onto a substrate;

attaching a semiconductor die to said substrate;

aligning an assembly over said semiconductor die, wherein said assembly comprises a heat sink and a thermally conductive element;

resting said assembly on said carrier such that said thermally conductive element does not directly contact said semiconductor die; and

encapsulating said thermally conductive element and said heat sink such that a portion of said heat sink is exposed to the surroundings of said package.